Utpal Bora

Ph.D. Scholar in Programming Languages and Compilers at IIT HYDERABAD

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Education

Aug 2014 – present — Integrated **M.Tech.** & **Ph.D. in Programming Languages and Compilers** in the *Dept. of Computer Science & Engineering* at IIT HYDERABAD (IITH), under the supervision of **Dr. Ramakrishna Upadrasta** and **Dr. Saurabh Joshi**.

Aug 2005 – Jul 2009 — **B.Tech.**, *Electronics & Communication Engineering*, DR. B. R. AMBEDKAR NATIONAL INSTITUTE OF TECHNOLOGY JALANDHAR (NIT Jalandhar).

Publications

Journal Articles

1. **Bora**, **U.**, Das, S., Kukreja, P., Joshi, S., Upadrasta, R., & Rajopadhye, S. (2020). LLOV: A Fast Static Data-Race Checker for OpenMP Programs. *ACM Trans. Archit. Code Optim.*, *17*(4). https://doi.org/10.1145/3418597
2. Jain, S., **Bora**, **U.**, Kumar, P., Sinha, V. B., Purini, S., & Upadrasta, R. (2019). An Analysis of Executable Size Reduction by LLVM Passes. *CSI Transactions on ICT*, *7*(2), 105–110. https://doi.org/10.1007/s40012-019-00248-5

Conference Proceedings

1. **Bora**, **U.**, Vaishay, S., Joshi, S., & Upadrasta, R. (2021). OpenMP aware MHP Analysis for Improved Static Data-Race Detection. *Proceedings of the Seventh Annual Workshop on the LLVM Compiler Infrastructure in HPC*. To be published.

Miscellaneous

1. **Bora**, **U.**, Das, S., Kukreja, P., Joshi, S., Upadrasta, R., & Rajopadhye, S. (2021). LLOV: A Fast Static Data-Race Checker for OpenMP Programs [Technical Talk, HiPEAC].
2. **Bora**, **U.**, Das, S., Kukreja, P., Joshi, S., Upadrasta, R., & Rajopadhye, S. (2020). LLOV: A Fast Static Data-Race Checker for OpenMP Programs [Technical Talk, LLVM Performance Workshop at CGO].
3. **Bora**, **U.**, Das, S., Kukreja, P., Joshi, S., Upadrasta, R., & Rajopadhye, S. (2020). LLOV: A Fast Static Data-Race Checker for OpenMP Programs [Technical Talk, RHPL Workshop at FSTTCS].
4. Kukreja, P., Shukla, H., & **Bora**, **U.** (2019). DataRaceBench FORTRAN [Open Source Benchmark, Github].
5. Dangeti, T. K., **Bora**, **U.**, Das, S., Grosser, T., & Upadrasta, R. (2017). Improved Loop Distribution in LLVM using Polyhedral Dependences [Lightning Talk, LLVM-HPC Workshop at SC].
6. **Bora**, **U.**, Doerfert, J., Grosser, T., & Upadrasta, R. (2016). GSoC 2016: PolyhedralInfo - Polly as an Analysis Pass in LLVM [Lightning Talk, US LLVM Dev Meet].
7. **Bora**, **U.**, & Pratik, B. (2016). Introduction to LLVM Compiler Infrastructure [Invited Talk, GDG DevFest Hyderabad].
8. Das, S., Kumar, D. T., **Bora**, **U.**, & Upadrasta, R. (2016). A Comparative Study of Vectorization in Compilers [Student Research Symposium, HiPC].

Projects

2017 **Loop Nest Optimization:** Developed an infrastructure in LLVM to perform loop nest optimizations (LNO) such as loop distribution, statement reordering, and loop vectorization using polyhedral reduced dependence graph. This work was presented in LLVM-HPC [8] at SC'17.

2019 **DRB FORTRAN:** Implemented a benchmark of OpenMP kernels in FORTRAN for data race detection. It contains kernels with data races and kernels without known races. The benchmark is released under open source licence (Github).

2021 **LLOV:** Developed LLOV- A Fast Static Data-Race Checker for OpenMP Programs [1]. The tool is available to download for free (Github).

Experience

Aug 2015 – Jan 2016 **Research Internship** at AMD India Pvt. Ltd. in the Compilers team. Worked on using Polyhedral program analysis in LLVM.

Dec 2009 – May 2014 **Software Developer** at DXC Technology (formerly CSC India Pvt. Ltd.): 4 years 6 month's work experience as application Software Developer. Worked on design and development of business applications for the insurance domain. Experience in C# for frontend and Microsoft SQL Server for backend development. Experience in all aspects of the application delivery lifecycle from business change initiation, design & build to deployment, test & operational support i.e end to end SDLC.

Recognition

Awards and Achievements

Feb 2020 Awarded a *student travel grant* by the ACM SIGPLAN to attend CGO 2020.

Aug 2018 Selected for the ECOOP/ISSTA '18 Summer School (with travel grant), Amsterdam, Netherlands. (Could not attend)

2016-17 Awarded *student travel grants* by the LLVM Foundation to attend the LLVM Developers' Meetings in 2016 & 2017.

June 2016 Successfully completed **Google Summer of Code** project *Polly as an Analysis Pass in LLVM* with the LLVM Compiler Infrastructure organization. GSoC Project, Blog.

Aug 2015 Awarded the **Visvesvaraya Ph.D. Fellowship**, (MeitY, India).

Jun 2015 Represented IIT Hyderabad in a research collaboration visit to Ritsumeikan University, Japan.

Mar 2015 Received the **Academic Excellence Certificate** for outstanding academic performance in the M.Tech. program at IIT Hyderabad.

May 2014 Secured All India Rank 239 among 155k applicants (**99.8% percentile**) in GATE-2014 examination in CS & IT branch having done B.Tech in ECE branch.

Oct 2010 Awarded **Star Performer of the Quarter** at CSC India Pvt. Ltd. for outstanding performance in Q3.

Committee and Volunteer-ship

Committee TPDS Reviewer, CGO'22 AEC, ASPLOS'22 AEC, MICRO'21 AEC, ASPLOS'21 AEC, PACT'21 AEC, ISSTA'21 AEC, ECOOP'21 AEC, SC'21 AD/AE, JSys AEB, IndoSys'19 Sub-reviewer

Student Volunteer SPLASH'21, PLDI'21, POPL'21, ICSE'21, ACCU'21, IndoSys'18

Teaching Experience

2015-2020 Teaching assistant for *Introduction to Programming*, *Data Structure and Programming*, *Principles of Programming Languages*, *Compiler Design*, *Compiler Engineering* (LLVM), *Compiler Optimizations*, and *Topics in Compiler Optimizations* courses at IIT Hyderabad.

2016-2020 Co-taught in *Compiler Engineering* courses at IIT Hyderabad using the LLVM Infrastructure.