CURRICULUM VITAE FOR BROOKS DAVIS

Principal Research Scientist
October 3, 2025

12 New Square
Cambridge
CB1 1EY
United Kingdom

+44 7883 473387
+1 206 383 8794
brooks@capabilitieslimited.co.uk
brooks@freebsd.org

EDUCATION

Bachelor of Science with Distinction and Honors, Computer Science, Harvey Mudd College, 1998.

PROFESSIONAL EXPERIENCE

Capabilities Limited

Principal Research Scientist (August 2025–present)

SRI International

Principal Computer Scientist February 2021–July 2025 (presently on leave)
Senior Software Engineer May 2012–January 2021

University of Cambridge

Visiting Industrial Fellow August 2013–present

The Aerospace Corporation

Senior Engineering Specialist, Technical Computing Services 2008–2012
Engineering Specialist, Computer System Research Department 1998–2008

The FreeBSD Project

Source Committer 2001–present
Ports Committer 2005–present
Core Team 2006–2012, 2018–2020

CheriBSD

Project lead 2012–present

FUNDING

Capabilities Limited, B. Davis (PI)). CheriBSD feature extraction, maturity, and testing. Innovate UK, Contracts for Innovation: DSbD Advancing CHERI Tools and software, Sept. 2025. Total: £981K, Contract: 10168042

SRI International, B. Davis (PI), P. Neumann (Co-PI). Deploying effective compartmentalization (DEC). DARPA I2O, Compartmentalization and Privilege Management (CPM), Mar. 2024. Total: $8.3M, Contract: FA875024CB047

SRI International, B. Davis (PI), P. Neumann (Co-PI). Memory and type safety at scale (MTSS). DARPA I2O, Office Wide BAA, Jan. 2023. Total: $1.5M, Contract: HR001123C0031

SRI International, P. Neumann (PI), B. Davis (Co-PI). DARPA I2O, Enabling Technologies for Compartmentalization (ETC), May 2022. Total: $3M, Contract: HR001122C0110

PROFESSIONAL SOCIETIES

Senior Member of the ACM and Member of the IEEE Computer Society.

PEER-REVIEWED JOURNAL AND MAGAZINE ARTICLES

R. N. Watson, J. Baldwin, D. Chisnall, T. Chen, J. Clarke, B. Davis, N. Filardo, B. Gutstein, G. Jenkinson, B. Laurie, A. Mazzinghi, S. Moore, P. G. Neumann, H. Okhravi, A. Richardson, A. Rebert, P. Sewell, L. Tratt, M. Vijayaraghavan, H. Vincent,

and K. Witaszczyk. It is time to standardize principles and practices for software memory safety. *Commun. ACM*, Jan. 2025. [PDF]

R. N. M. Watson, D. Chisnall, J. Clarke, B. Davis, N. W. Filardo, B. Laurie, S. W. Moore, P. G. Neumann, A. Richardson, P. Sewell, K. Witaszczyk, and J. Woodruff. CHERI: Hardware-enabled C/C++ memory protection at scale. *IEEE Security & Privacy*, 22(4):50–61, 2024. (**Best paper**.) [IEEE]

J. Woodruff, A. Joannou, H. Xia, A. Fox, R. M. Norton, D. Chisnall, B. Davis, K. Gudka, N. W. Filardo, A. T. Markettos, M. Roe, P. G. Neumann, R. N. M. Watson, and S. W. Moore. CHERI concentrate: Practical compressed capabilities. *IEEE Transactions on Computers*, 68(10):1455–1469, 2019. [PDF]

R. N. Watson, R. M. Norton, J. Woodruff, S. W. Moore, P. G. Neumann, J. Anderson, D. Chisnall, B. Davis, B. Laurie, M. Roe, N. H. Dave, K. Gudka, A. Joannou, A. T. Markettos, E. Maste, S. J. Murdoch, C. Rothwell, S. D. Son, and M. Vadera. Fast protection-domain crossing in the CHERI capability-system architecture. *IEEE Micro*, 36(5):38–49, 2016. [PDF]

PEER-REVIEWED CONFERENCE PAPERS

F. A. Fuchs, J. Woodruff, P. Rugg, A. Joannou, J. Clarke, J. Baldwin, B. Davis, P. G. Neumann, R. N. M. Watson, and S. W. Moore. Safe speculation for CHERI. In *2024 IEEE 42st International Conference on Computer Design (ICCD)*, 2024. [PDF]

N. W. Filardo, B. F. Gutstein, J. Woodruff, J. Clarke, P. Rugg, B. Davis, M. Johnston, R. Norton, D. Chisnall, S. W. Moore, P. G. Neumann, and R. N. M. Watson. Cornucopia reloaded: Load barriers for CHERI heap temporal safety. In *Proceedings of the 29th ACM International Conference on Architectural Support for Programming Languages and Operating Systems, Volume 2*, ASPLOS '24, page 251–268, New York, NY, USA, 2024. Association for Computing Machinery. (18.4% acceptance) [PDF]

V. Zaliva, K. Memarian, R. Almeida, J. Clarke, B. Davis, A. Richardson, D. Chisnall, B. Campbell, I. Stark, R. N. M. Watson, and P. Sewell. Formal mechanised semantics of CHERI C: Capabilities, undefined behaviour, and provenance. In *Proceedings of the 29th ACM International Conference on Architectural Support for Programming Languages and Operating Systems, Volume 1*, ASPLOS '24, page 181–196, New York, NY, USA, 2024. Association for Computing Machinery. [PDF]

F. A. Fuchs, J. Woodruff, P. Rugg, M. van der Maas, A. Joannou, A. Richardson, J. Clarke, N. W. Filardo, B. Davis, J. Baldwin, P. G. Neumann, S. W. Moore, and R. N. M. Watson. Architectural contracts for safe speculation. In *2023 IEEE 41st International Conference on Computer Design (ICCD)*, pages 578–586, 2023. (39% acceptance) [PDF]

B. Davis. So you want to add a system call? In *Proceedings of AsiaBSDCon 2023*, Tokyo, Japan, Apr. 2023

N. Wesley Filardo, B. F. Gutstein, J. Woodruff, S. Ainsworth, L. Paul-Trifu, B. Davis, H. Xia, E. Tomasz Napierala, A. Richardson, J. Baldwin, D. Chisnall, J. Clarke, K. Gudka, A. Joannou, A. Theodore Markettos, A. Mazzinghi, R. M. Norton, M. Roe, P. Sewell, S. Son, T. M. Jones, S. W. Moore, P. G. Neumann, and R. N. M. Watson. Cornucopia: Temporal safety for CHERI heaps. In *2020 IEEE Symposium on Security and Privacy ("Oakland" 2020))*, pages 608–625, San Jose, CA, USA, May 2020. (11% acceptance) [PDF]

B. Davis, R. N. M. Watson, A. Richardson, P. G. Neumann, S. W. Moore, J. Baldwin, D. Chisnall, J. Clarke, N. W. Filardo, K. Gudka, A. Joannou, B. Laurie, A. T. Markettos, J. E. Maste, A. Mazzinghi, E. T. Napierala, R. M. Norton, M. Roe, P. Sewell, S. Son, and J. Woodruff. CheriABI: Enforcing valid pointer provenance and minimizing pointer privilege in the POSIX C run-time environment. In *Proceedings of the Twenty-Fourth International Conference on Architectural Support for Programming Languages and Operating Systems*, ASPLOS '19, page 379–393, New York, NY, USA, 2019. Association for Computing Machinery. (**Best paper**. 21% acceptance) [PDF, Tech Report]

K. Memarian, V. B. F. Gomes, B. Davis, S. Kell, A. Richardson, R. N. M. Watson, and P. Sewell. Exploring C semantics and pointer provenance. *Proceedings of the ACM on Programming Languages*, 3(POPL), Jan. 2019. (29% acceptance), [PDF]

H. Xia, J. Woodruff, H. Barral, L. Esswood, A. Joannou, R. Kovacsics, D. Chisnall, M. Roe, B. Davis, E. Napierala, J. Baldwin, K. Gudka, P. G. Neumann, A. Richardson, S. W. Moore, and R. N. M. Watson. CheriRTOS: A capability model for embedded devices. In *2018 IEEE 36th International Conference on Computer Design (ICCD)*, pages 92–99, 2018. (29% acceptance) [PDF]

A. Joannou, J. Woodruff, R. Kovacsics, S. W. Moore, A. Bradbury, H. Xia, R. N. Watson, D. Chisnall, M. Roe, B. Davis, E. Napierala, J. Baldwin, K. Gudka, P. G. Neumann, A. Mazzinghi, A. Richardson, S. Son, and A. T. Markettos. Efficient tagged memory. In *2017 IEEE International Conference on Computer Design (ICCD)*, pages 641–648, 2017. (29% acceptance) [PDF]

D. Chisnall, B. Davis, K. Gudka, D. Brazdil, A. Joannou, J. Woodruff, A. T. Markettos, J. E. Maste, R. Norton, S. Son, M. Roe, S. W. Moore, P. G. Neumann, B. Laurie, and R. N. Watson. CHERI JNI: Sinking the Java security model into the C. In *Proceedings of the Twenty-Second International Conference on Architectural Support for Programming Languages and Operating Systems*, ASPLOS '17, page 569–583, New York, NY, USA, 2017. Association for Computing Machinery. (17% acceptance) [PDF]

B. Davis. Everything you ever wanted to know about "hello, world."* (*but were afraid to ask.). In *Proceedings of AsiaBSDCon 2017*, Tokyo, Japan, Mar. 2017. [PDF]

K. Gudka, R. N. Watson, J. Anderson, D. Chisnall, B. Davis, B. Laurie, I. Marinos, P. G. Neumann, and A. Richardson. Clean application compartmentalization with SOAAP. In *Proceedings of the 22nd ACM SIGSAC Conference on Computer and Communications Security*, CCS '15, page 1016–1031, New York, NY, USA, 2015. Association for Computing Machinery. (20% acceptance) [PDF]

R. N. Watson, J. Woodruff, P. G. Neumann, S. W. Moore, J. Anderson, D. Chisnall, N. Dave, B. Davis, K. Gudka, B. Laurie, S. J. Murdoch, R. Norton, M. Roe, S. Son, and M. Vadera. CHERI: A hybrid capability-system architecture for scalable software compartmentalization. In *2015 IEEE Symposium on Security and Privacy ("Oakland")*, pages 20–37, 2015. (**Test of time award, IEEE S&P 2025.** 14% acceptance) [PDF]

D. Chisnall, C. Rothwell, R. N. Watson, J. Woodruff, M. Vadera, S. W. Moore, M. Roe, B. Davis, and P. G. Neumann. Beyond the PDP-11: Architectural support for a memory-safe C abstract machine. In *Proceedings of the Twentieth International Conference on Architectural Support for Programming Languages and Operating Systems*, ASPLOS '15, page 117–130, New York, NY, USA, 2015. Association for Computing Machinery. (17% acceptance) [PDF]

J. Woodruff, R. N. Watson, D. Chisnall, S. W. Moore, J. Anderson, B. Davis, B. Laurie, P. G. Neumann, R. Norton, and M. Roe. The CHERI capability model: revisiting RISC in an age of risk. In *Proceeding of the 41st Annual International Symposium on Computer Architecuture*, ISCA '14, page 457–468. IEEE Press, 2014. (17% acceptance) [PDF]

J. Anderson, R. N. M. Watson, D. Chisnall, K. Gudka, I. Marinos, and B. Davis. TESLA: temporally enhanced system logic assertions. In *Proceedings of the Ninth European Conference on Computer Systems*, EuroSys '14, New York, NY, USA, 2014. Association for Computing Machinery. (18% acceptance) [PDF]

B. Davis, R. Norton, J. Woodruff, and R. N. M. Watson. How FreeBSD boots: a soft-core MIPS perspective. In *Proceedings of AsiaBSDCon 2014*, Tokyo, Japan, Mar. 2014. [PDF]

A. T. Markettos, J. Woodruff, R. N. M. Watson, B. A. Zeeb, B. Davis, and S. W. Moore. The BERIpad tablet: open-source construction, CPU, OS and applications. In *Proceedings of FPGA Workshop and Design Contest*, Southeast University, Nanjing, China, Nov. 2013

B. Davis. Improving system management with ZFS. In *Proceedings of AsiaBSDCon 2011*, Tokyo, Japan, Mar. 2011

B. Davis. Porting high performance computing tools to FreeBSD. In *Proceedings of AsiaBSDCon 2010*, Tokyo, Japan, Mar. 2010

B. Davis. Isolating cluster jobs for performance and predictability. In *Proceedings of AsiaBSDCon 2009*, Tokyo, Japan, Mar. 2009

B. Davis. Using FreeBSD to promote open source development methods. In *Proceedings of AsiaBSDCon 2008*, Tokyo, Japan, Mar. 2008

T. Barr, C. Byron, Z. Duron, R. Keller, B. Lickly, C. Nygaard, K. Roberts, M. AuYeung, J. Betser, J. Coggi, B. Davis, C. Lee, D. Stodden, and M. Thomas. Grid-enabling orbital analysis and computationally intensive applications for a growing set of diversified users. In *NOMS 2008 - 2008 IEEE Network Operations and Management Symposium*, pages 615–629, 2008. [IEEE]

B. Davis, M. AuYeung, J. M. Clark, C. Lee, J. Palko, and M. Thomas. Reflections on building a high-performance computing cluster using FreeBSD. In *Proceedings of AsiaBSDCon 2007*, Tokyo, Japan, Mar. 2007. [PDF]

B. Davis, M. AuYeung, M. Clark, C. Lee, M. Thomas, J. Palko, and R. Varney. Lessons learned building a general purpose cluster for space mission applications. In *2nd IEEE International Conference on Space Mission Challenges for Information Technology (SMC-IT'06)*, pages 9 pp.–, 2006

B. Davis. The challenges of dynamic network interfaces. In *Proceedings of EuroBSDCon 2004*, Karlsruhe, Germany, Oct. 2004

B. Davis, M. AuYeung, G. Green, and C. Lee. Building a high-performance computing cluster using FreeBSD. In *BSDCon 2003*, San Mateo, CA, Sept. 2003. USENIX Association

C. Lee, E. Coe, B. Michel, J. Stepanek, I. Solis, J. Clark, and B. Davis. Using topology-aware communication services in grid environments. In *CCGrid 2003. 3rd IEEE/ACM International Symposium on Cluster Computing and the Grid, 2003. Proceedings.*, pages 534–541, 2003

C. Lee, E. Coe, J. Clark, and B. Davis. Managing advanced communication services using active network overlays in grid environments. In *Proceedings of Fourth Annual International Workshop on Active Middleware Services*, pages 11–18, 2002

OTHER PEER-REVIEWED PRESENTATIONS AND PUBLICATIONS

B. Davis. Address space reservations: Re-thinking address space management for pointer provenance. EuroBSDCon 2024, Dublin, Ireland, Sept. 2024

B. Davis. Address space reservations: Re-thinking address space management for pointer provenance. BSDCan 2024, Ottawa, Canada, May 2024

B. Davis. Creating a memory-safe workstation with CheriBSD. BSDCan 2023, Ottawa, Canada, May 2023

B. Davis. CHERI & ZFS. OpenZFS Developer Summit 2022, San Francisco, CA, USA, Oct. 2022

B. Davis. So you want to add a system call? EuroBSDCon 2022, Vienna, Austria, Sept. 2022

B. Davis. So you want to add a system call? BSDCan 2022, Virtual, June 2022

B. Davis. CheriBSD: A memory safe POSIX OS. FOSDEM 2021, Virtual, Feb. 2021

B. Davis. CheriABI: Hardware enforced memory safety for FreeBSD. EuroBSDCon 2019, Lillehammer, Norway, Sept. 2019

B. Davis. Is it time to replace mmap? BSDTW 2017, Taipei, Taiwan, Nov. 2017

B. Davis. Everything you ever wanted to know about ”hello, world.”* (*but were afraid to ask. EuroBSDCon 2016, Belgrade, Serbia, Sept. 2016

B. Davis. Everything you ever wanted to know about ”hello, world.”* (*but were afraid to ask. BSDCan 2016, Ottawa, Canada, June 2016

B. Davis. CheriBSD: A research fork of FreeBSD. BSDCan 2015, Ottawa, Canada, June 2015

B. Davis. Improving system management with ZFS. BSDCan 2011, Ottawa, Canada, May 2011

B. Davis. Improving system management with ZFS. EuroBSDCon 2011, Maarssen, The Netherlands, Oct. 2011

B. Davis. Porting high performance computing tools to FreeBSD. BSDCan 2010, Ottawa, Canada, May 2010

B. Davis. Porting high performance computing tools to FreeBSD. EuroBSDCon 2009, Cambridge, UK, Sept. 2009

B. Davis. Isolating cluster jobs for performance and predictability. BSDCan 2009, Ottawa, Canada, May 2009

B. Davis. Isolating cluster jobs for performance and predictability. EuroBSDCon 2008, Strasbourg, France, Oct. 2008

B. Davis. Using FreeBSD to promote open source development methods. BSDCan 2008, Ottawa, Canada, May 2008

B. Davis. Using FreeBSD to promote open source development methods. EuroBSDCon 2007, Copenhagen, Denmark, May 2007

INVITED PRESENTATIONS

B. Davis. Keynote: The long road to hardware-enforced memory safety. EuroSec 2023, Rome, Italy, May 2023

B. Davis. Everything you ever wanted to know about ”hello, world.”* (*but were afraid to ask. FOSDEM 2017 (main track), Brussels, Belgium, Mar. 2017

B. Davis. Keynote: Promoting open source methods at a large company. FOSDEM 2010. Brussels, Belgium, Feb. 2010

TUTORIALS

B. Davis. Building clusters with FreeBSD. EuroBSDCon 2007, Copenhagen, Denmark, May 2007

B. Davis. Building clusters with FreeBSD. AsiaBSDCon 2007, Tokyo, Japan, Mar. 2007

B. Davis. Building clusters with FreeBSD. EuroBSDCon 2006, Milan, Italy, Nov. 2006

B. Davis. Building clusters with FreeBSD. BSDCan 2006, Ottawa, Canada, May 2006

INVITED PUBLICATIONS

B. Davis. A dozen years of CheriBSD. *The FreeBSD Journal (FreeBSD 30th Anniversary Edition)*, May-June 2023. [PDF]

B. Davis. Improving memory permissions in FreeBSD. *The FreeBSD Journal*, November-December 2019

B. Davis. CHERI: Building a foundation for secure trusted computing bases. *The FreeBSD Journal*, March-April 2016

B. Davis, R. Norton, and R. N. M. Watson. Bringing up MIPS. *The FreeBSD Journal*, January-February 2015

TECHNICAL REPORTS AND STANDARDS

R. N. M. Watson, J. Baldwin, T. Chen, D. Chisnall, J. Clarke, B. Davis, N. W. Filardo, B. Gutstein, G. Jenkinson, B. Laurie, A. Mazzinghi, S. W. Moore, P. G. Neumann, H. Okhravi, A. Rebert, A. Richardson, P. Sewell, L. Tratt, M. Vijayaraghavan, H. Vincent, and K. Witaszczyk. It's time to standardize principles and practices for software memory safety (full report). Technical Report UCAM-CL-TR-996, University of Cambridge, Computer Laboratory, 15 JJ Thomson Avenue, Cambridge CB3 0FD, United Kingdom, phone +44 1223 763500. (To appear) [PDF]

T. Aird, H. Almatary, A. A. Garcia, J. Baldwin, P. Buxton, D. Chisnall, J. Clarke, B. Davis, N. W. Filardo, F. A. Fuchs, T. Hutt, A. Joannou, M. Kaiser, T. Kurd, B. Laurie, M. van der Maas, M. Malenko, A. T. Markettos, D. McKay, J. Melling, S. Menefy, S. W. Moore, P. G. Neumann, R. Norton, A. Richardson, M. Roe, P. Rugg, P. Sewell, C. Shaw, R. Tura, R. N. M. Watson, T. Wenman, J. Woodruff, and J. Z. Yu. *RISC-V Specification for CHERI Extensions (v0.9.7 Draft)*. Oct. 2025. [PDF]

V. Zaliva, K. Memarian, R. Almeida, J. Clarke, B. Davis, A. Richardson, D. Chisnall, B. Campbell, I. Stark, R. N. M. Watson, and P. Sewell. CHERI C semantics as an extension of the ISO C17 standard. Technical Report UCAM-CL-TR-988, University of Cambridge, Computer Laboratory, Oct. 2023. [PDF]

R. N. M. Watson, P. G. Neumann, J. Woodruff, M. Roe, H. Almatary, J. Anderson, J. Baldwin, G. Barnes, D. Chisnall, J. Clarke, B. Davis, L. Eisen, N. W. Filardo, F. A. Fuchs, R. Grisenthwaite, A. Joannou, B. Laurie, A. T. Markettos, S. W. Moore, S. J. Murdoch, K. Nienhuis, R. Norton, A. Richardson, P. Rugg, P. Sewell, S. Son, and H. Xia. Capability Hardware Enhanced RISC Instructions: CHERI Instruction-Set Architecture (Version 9). Technical Report UCAM-CL-TR-987, University of Cambridge, Computer Laboratory, Sept. 2023. Current ISA version, basis for RV64Y. [PDF]

R. N. M. Watson, P. G. Neumann, J. Woodruff, M. Roe, H. Almatary, J. Anderson, J. Baldwin, G. Barnes, D. Chisnall, J. Clarke, B. Davis, L. Eisen, N. W. Filardo, R. Grisenthwaite, A. Joannou, B. Laurie, A. T. Markettos, S. W. Moore, S. J. Murdoch, K. Nienhuis, R. Norton, A. Richardson, P. Rugg, P. Sewell, S. Son, and H. Xia. Capability Hardware Enhanced RISC Instructions: CHERI Instruction-Set Architecture (Version 8). Technical Report UCAM-CL-TR-951, University of Cambridge, Computer Laboratory, Oct. 2020. Synchronized with Arm's Morello prototype. [PDF]

R. N. M. Watson, A. Richardson, B. Davis, J. Baldwin, D. Chisnall, J. Clarke, N. Filardo, S. W. Moore, E. Napierala, P. Sewell, and P. G. Neumann. CHERI C/C++ Programming Guide. Technical Report UCAM-CL-TR-947, University of Cambridge, Computer Laboratory, June 2020. [PDF]

B. Davis, R. N. M. Watson, A. Richardson, P. G. Neumann, S. W. Moore, J. Baldwin, D. Chisnall, J. Clarke, N. W. Filardo, K. Gudka, A. Joannou, B. Laurie, A. T. Markettos, J. E. Maste, A. Mazzinghi, E. T. Napierala, R. M. Norton, M. Roe, P. Sewell, S. Son, and J. Woodruff. CheriABI: Enforcing valid pointer provenance and minimizing pointer privilege in the POSIX C run-time environment. Technical Report UCAM-CL-TR-932, University of Cambridge, Computer Laboratory, Apr. 2019

R. N. M. Watson, P. G. Neumann, J. Woodruff, M. Roe, H. Almatary, J. Anderson, J. Baldwin, D. Chisnall, B. Davis, N. W. Filardo, A. Joannou, B. Laurie, A. T. Markettos, S. W. Moore, S. J. Murdoch, K. Nienhuis, R. Norton, A. Richardson, P. Rugg, P. Sewell, S. Son, and H. Xia. Capability Hardware Enhanced RISC Instructions: CHERI Instruction-Set Architecture (Version 7). Technical Report UCAM-CL-TR-927, University of Cambridge, Computer Laboratory, June 2019

R. N. M. Watson, P. G. Neumann, J. Woodruff, M. Roe, J. Anderson, J. Baldwin, D. Chisnall, B. Davis, A. Joannou, B. Laurie, S. W. Moore, S. J. Murdoch, R. Norton, S. Son, and H. Xia. Capability Hardware Enhanced RISC Instructions: CHERI Instruction-Set Architecture (Version 6). Technical Report UCAM-CL-TR-907, University of Cambridge, Computer Laboratory, Apr. 2017

R. N. M. Watson, P. G. Neumann, J. Woodruff, M. Roe, J. Anderson, D. Chisnall, B. Davis, A. Joannou, B. Laurie, S. W. Moore, S. J. Murdoch, R. Norton, S. Son, and H. Xia. Capability Hardware Enhanced RISC Instructions: CHERI Instruction-Set Architecture (Version 5). Technical Report UCAM-CL-TR-891, University of Cambridge, Computer Laboratory, June 2016

R. N. M. Watson, D. Chisnall, B. Davis, W. Koszek, S. W. Moore, S. J. Murdoch, P. G. Neumann, and J. Woodruff. Capability Hardware Enhanced RISC Instructions: CHERI Programmer's Guide. Technical Report UCAM-CL-TR-877, University of Cambridge, Computer Laboratory, Sept. 2015

R. N. M. Watson, P. G. Neumann, J. Woodruff, M. Roe, J. Anderson, D. Chisnall, B. Davis, A. Joannou, B. Laurie, S. W. Moore, S. J. Murdoch, R. Norton, and S. Son. Capability Hardware Enhanced RISC Instructions: CHERI Instruction-Set Architecture. Technical Report UCAM-CL-TR-876, University of Cambridge, Computer Laboratory, Sept. 2015

K. Gudka, R. N. Watson, J. Anderson, D. Chisnall, B. Davis, B. Laurie, I. Marinos, P. G. Neumann, and A. Richardson. Clean application compartmentalization with SOAAP (extended version). Technical Report UCAM-CL-TR-873, University of Cambridge, Computer Laboratory, Aug. 2015

R. N. M. Watson, D. Chisnall, B. Davis, W. Koszek, S. W. Moore, S. J. Murdoch, P. G. Neumann, and J. Woodruff. Bluespec Extensible RISC Implementation: BERI Software reference. Technical Report UCAM-CL-TR-869, University of Cambridge, Computer Laboratory, Apr. 2015

R. N. M. Watson, J. Woodruff, D. Chisnall, B. Davis, W. Koszek, A. T. Markettos, S. W. Moore, S. J. Murdoch, P. G. Neumann, R. Norton, and M. Roe. Bluespec Extensible RISC Implementation: BERI Hardware reference. Technical Report UCAM-CL-TR-868, University of Cambridge, Computer Laboratory, Apr. 2015

R. N. M. Watson, P. G. Neumann, J. Woodruff, J. Anderson, D. Chisnall, B. Davis, B. Laurie, S. W. Moore, S. J. Murdoch, and M. Roe. Capability Hardware Enhanced RISC Instructions: CHERI Instruction-set architecture. Technical Report UCAM-CL-TR-864, University of Cambridge, Computer Laboratory, Dec. 2014

R. N. Watson, D. Chisnall, B. Davis, W. Koszek, S. W. Moore, S. J. Murdoch, P. G. Neumann, and J. Woodruff. Bluespec Extensible RISC Implementation: BERI Software reference. Technical Report UCAM-CL-TR-853, University of Cambridge, Computer Laboratory, Apr. 2014

R. N. Watson, J. Woodruff, D. Chisnall, B. Davis, W. Koszek, A. T. Markettos, S. W. Moore, S. J. Murdoch, P. G. Neumann, R. Norton, and M. Roe. Bluespec Extensible RISC Implementation: BERI Hardware reference. Technical Report UCAM-CL-TR-852, University of Cambridge, Computer Laboratory, Apr. 2014

R. N. Watson, D. Chisnall, B. Davis, W. Koszek, S. W. Moore, S. J. Murdoch, P. G. Neumann, and J. Woodruff. Capability Hardware Enhanced RISC Instructions: CHERI User's guide. Technical Report UCAM-CL-TR-851, University of Cambridge, Computer Laboratory, Apr. 2014

R. N. Watson, P. G. Neumann, J. Woodruff, J. Anderson, D. Chisnall, B. Davis, B. Laurie, S. W. Moore, S. J. Murdoch, and M. Roe. Capability Hardware Enhanced RISC Instructions: CHERI Instruction-set architecture. Technical Report UCAM-CL-TR-850, University of Cambridge, Computer Laboratory, Apr. 2014

Security Advisories

B. Davis. Possible login(1) argument injection in telnetd(8). CVE-2016-1888, FreeBSD-SA-16:36.telnetd, Dec. 2016